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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,947	10/30/2000	Edmund J. Kelly	TRANS04D	8830

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TRANSMETA C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/699,947	KELLY ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3, 18 and 20-28* is/are pending in the application.

4a) Of the above claim(s) *2,4-17 and 19* is/are withdrawn from consideration.

5)☒ Claim(s) *18,20 and 26-28* is/are allowed.

6)☒ Claim(s) *1,3,21 and 23* is/are rejected.

7)☒ Claim(s) *22,24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/26/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Part III DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicant's communication filed May 26, 2009. This amendment has been entered and carefully considered. Claims 1, 3, 18 and 20-28 are presented for examination and pending in the application. Claims 2, 4-17 and 19 have been cancelled.

2. Applicant's arguments filed May 26, 2009 with respect to the pending claims 1 and 3 have been considered; however they are not being persuasive.

Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugimoto Koichi (Jap. App. No. 02-054058); hereinafter Koichi, in view of Moore et al. (USPN: 5,437,017); hereinafter Moore.

As per claims 1 and 3; Kochi discloses the invention as claimed including a system for maintaining translation consistency in a computer which includes a host processor (abstract) designed to execute instructions of a host instruction set and software (embedded in the system of Koichi) for translating instructions from a target instruction set to instructions of the host instruction set (abstract) comprises a hardware means comprises a look-aside buffer (TLB) 3 with an instruction converting unit 2 (e.g. see attached figure) for translating a first address storing a target instruction to a second memory address for use by the host having plurality of storage locations for virtual addresses and associated physical addresses and storage position in each storage location of the TLB (e.g. see attached figure); the software means is known to be embedded in the system of Koichi, particularly considered to be within the instruction converting unit 3, for carrying-out the translating/converting process. Koichi with only one exception does not particularly teaches the software means for

removing the at least one host instruction from the second memory address (claim 1), or invalidating the at least one host instruction at the second memory address (claim 3) for maintaining data consistency within the system. Moore, in his teaching of method and system for maintaining TLB coherency in a multiprocessor data processing system, discloses in maintaining data coherency between all translation look-aside-buffers, (a) the software synchronization is implemented throughout the multiprocessor data processing system; particularly, issuing the translation lookaside buffer invalidate (TLBI) instruction at all processors within the system (claim 3) (e.g. see column 2, lines 36-37; column 3, lines 12-27; figure 5, column 8, lines 32 et seq.), wherein the removing of the at least one host instruction at the second address is being equivalently taught as terminating the execution of all pending instructions (including host instruction) until after the TLBI instruction has been executed, or suspending execution of all pending instructions until all read and write operations within the memory queue have achieved coherency (e.g. see column 3, lines 19-27). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the software synchronization and invalidation of data/instruction in a multiprocessing environment as taught by

Moore for that of Koichi's system in order to arrive at Applicant's current invention. By removing and invalidating the host instruction from the second memory address, particularly when there is an update or modification of data/instruction within the system, it would prevent other processors or I/O units from executing stale or out-of-date instruction/data; thereby data coherency can be uniformly maintained, therefore being greatly advantageous.

As per claim 21, wherein the indication comprises a first bit value associated with each of the storage locations in the look-aside buffer (e.g. see Koichi's attached figure; and Abstract's constitution).

As per claim 23, the further limitation of "the host processor is a very long instruction word processor and wherein the target instructions comprise x86 instructions" is embedded and taught by Koichi and Moore to the extent that it is being claimed, since word processor and x86 instruction are notorious old and known in the memory storage art, and both Koichi and Moore are known to be operable with those claimed features (e.g. see Koichi's attached figure; and Abstract's constitution; Moore's abstract; column 6, lines 3 et seq.; column 10, lines 48 et seq.).

Allowable subject matter

5. Claims 22, 24-25 are objected to as being dependent upon a rejected based claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 18 is allowed. Claims 20 and 26-28 are also allowable since it is depended on the indicated allowable claim 18.

Response to Arguments

6. With respect to the remark, Applicant's counsels argued that Koichi and Moore do not show or suggest "means for providing an indication whether the first memory address to be written stores a target instruction which has been translated to at least one host instruction that is stored at a second memory address" (pages 7 and 8).

Examiner disagrees with the Applicant's counsel and would like to emphasize that the contended means for providing an indication whether the first memory address to be written stores a target instruction which has been translated to at least one host instruction that is stored at a second memory address is embedded in the system of Koichi and being taught to the extent that it is being claimed; for example, Koichi clearly discloses

translation look-aside buffer (TLB) 3 with an instruction converting unit 2 (e.g. see Koichi's attached figure) for translating a first address storing a target instruction to a second memory address for use by the host having plurality of storage locations for virtual addresses and associated physical addresses and storage position in each storage location of the TLB (e.g. see Abstract's constitution). With regarding to Moore reference, Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). Koichi and Moore references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969. In this case, the Moore reference was used to provide evidence of the well known concept of software synchronization and invalidation of data/instruction in a multiprocessing environment for removing and invalidating the host instruction from the second

memory address, particularly when there is an update or modification of data/instruction within the system in order to prevent other processors or I/O units from executing stale or out-of-date instruction/data; thereby data coherency can be uniformly maintained (e.g. see Moore's column 2, lines 36-37; column 3, lines 12-27; figure 5, column 8, lines 32 et seq.). Therefore, the 103 rejection based on the combination of Koichi and Moore reference in order to arrive at Applicant's current invention is deemed to be proper. In addition, Examiner would like to emphasize that in considering a 35 USC 103 rejection, it is not strictly necessary that a reference or references explicitly suggest the claimed invention (this is tantamount to a 35 USC 102 reference if the modifications would have been obvious to those of ordinary skill in the art. It has been held that the test of obviousness is not whether the features of a secondary reference may be bodily incorporated into the primary references' structure, nor whether the claimed invention is expressly suggested in any one or all of the references; rather, the test is what the combined teachings of the reference would have suggested to those of ordinary skill in the art. See In re Keller et al., 208 U.S.P.Q 871.

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-41287. The examiner can normally be reached from 6:30 A.M. to 3:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Sanjiv Shah can be reached on (571)-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-9300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information

about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/August 10, 2009

/Tuan V. Thai/
Primary Examiner, Art Unit 2185